

Appl. No.: 10/772,777
Amdt. Dated August 4, 2005
Reply to Office Action Dated May 4, 2005

REMARKS

Claims 1-25 are pending in the application. Claims 1, 3, and 14-25 have been amended. Claim 2 has been cancelled. Support for the amendments may be found throughout the specification, and particularly at pages 6-8. No new matter has been added. Applicants respectfully request favorable consideration and earnestly solicit allowance of the application in light of the above amendments and following remarks.

Objections to the Specification, and Claims

The objections to the specification and claims have been obviated by appropriate amendment.

Rejections Pursuant 35 U.S.C. § 102

Claims 1, 8-12, 16, 17 and 21 have been rejected under 35 U.S.C. 102(e) as being anticipated by *You et al.* (U.S. Pat No. 6,663,787), and claims 1, 2, 8-12 16, 17, and 21 have been rejected under 35 U.S.C. 102(b) as being anticipated by *Layadi et al.* (U.S. Pat No. 6,180,518). Applicants respectfully submit that neither *You* nor *Layadi* disclose the limitations of the pending claims.

Independent claim 1 relates to a method of fabricating a semiconductor integrated circuit including reactive ion etching a dielectric portion, within a dielectric etch chamber to produce a feature having sidewalls and a bottom. A metallic liner is produced on both the sidewalls and the bottom of the etched feature the during the reactive ion etching to form a metal-lined feature. Independent claim 17 relates to a method of fabricating a semiconductor integrated circuit where a metallic liner is formed in the etch chamber to provide a metallic liner on the sidewalls and the bottom of the feature etched in the dielectric during a reactive ion etching. In claims 1 and 17, the etching of the dielectric portion includes reactive ion etching that produces, during a reactive ion etching (claim 1), or in a reactive ion etching chamber (claim 17), to produce a metallic liner on both the sidewalls and the bottom of the etched feature.

The cited reference to *You*, on the other hand, does not disclose or suggest the limitations of the pending claims. Instead, *You* relates to use of TA/TAN for preventing copper

contamination of low-k dielectric layers. In *You*, a reverse sputtering process etches through a first diffusion barrier layer to expose the first metallization layer. (Figure 4E, col. 15, ll. 12-14). During sputtering of a first diffusion barrier layer, material of the first diffusion barrier layer liberated during the sputtering process is deposited on the sidewalls of the via to form a sidewall diffusion barrier layer. (Col. 15, ll. 19-22). Accordingly, *You* describes a reverse sputtering process that produces only a sidewall diffusion barrier layer. *You* does not disclose or suggest reactive ion etching to produce the feature, or a metal liner on both the sidewalls and bottom of the feature.

The cited reference to *Layadi* also does not disclose or suggest the limitations of independent claims 1 and 17. *Layadi* relates to methods for forming vias in low-k dielectric material. In the method of *Layadi*, a via is formed through a dielectric layer on an etch stop layer. (Figures 3 and 4; col. 3, ll. 25-27). After the dielectric layer has been etched to expose an upper surface of an etch stop layer, the exposed etch stop layer is etched with an etchant that cooperates with the etched material from the etch stop layer to form a polymeric layer to coat the porous sidewalls of the via. (Col. 4, ll. 35-39) The etchant etches away the etch stop layer to form the polymeric layer on the sidewalls of the via. (Col. 4, ll. 39-43). Accordingly, *Layadi* describes etching a via to form a polymeric layer, and that polymeric layer is produced only on a sidewall of a via. *Layadi* does not disclose or suggest that both the bottom and the sidewalls are lined. Moreover, *Layadi* does not disclose or suggest producing a metal-lined feature.

Both *You* and *Layadi* disclose arrangements where only sidewalls are lined. Neither discloses or suggests producing within a dielectric etch chamber, a desired reactive ion etched profile, while using a metallic redeposition to produce a metallic liner on both the sidewalls and the bottom of the etched feature. Clearly, neither *You* nor *Layadi* disclose that a metal liner can be formed as in claims 1 and 17 during a reactive ion etching, in a reactive ion etching chamber. Accordingly, limitations of independent claims 1 and 17 are entirely missing in the cited art.

Claims 3-16 and 18-21

Applicants also respectfully submit that dependent claims 3-15 and 18-20 are not anticipated by the cited art. As discussed, limitations for independent claims 1 and 17 are not

disclosed by the cited art. Therefore, the limitations of the claims dependent therefrom are also not disclosed or fairly suggested by the cited combination. Claims 16 and 21 have been re-written in independent form and recite structural limitations not disclosed in the cited art, as discussed above for claims 1 and 17 respectively. Accordingly, Applicants respectfully submit that claims 3-16 and 18-21 are not anticipated.

Rejections Pursuant 35 U.S.C. § 103

Claim 13 has been deemed obvious over *Layadi* in view of *Lin et al.* (U.S. Pat. No. 6,743,732), claims 14, 15, 19 and 20 are deemed obvious over *Layadi*, and claims 2-7, 18 and claims 22-25 are deemed obvious over *You* in view of *Dalton et al.* (U.S. 200110036753).

Claims 2-7, 13-15, 19 and 20 dependent from claims 1 and 17. Independent claim 22 relates to a method of fabricating a semiconductor integrated circuit where a reactive ion etching is performed on a low-k dielectric portion, within a dielectric etch chamber to produce a feature having a metallic liner both sidewalls and a bottom of the etched feature. Independent claim 24 also relates to a method of fabricating a semiconductor integrated circuit where a metallic liner is produced in an etched feature in a low-k dielectric portion, where the metallic liner is produced on the sidewalls and the bottom of the feature in an etch chamber. Like independent claims 1 and 17, in independent claims 22 and 24, the etching of the dielectric portion includes reactive ion etching that produces, during a reactive ion etching (claim 22), or in an etching chamber (claim 24), a conformal metallic liner on both the sidewalls and the bottom of the etched feature.

As discussed, both *You* and *Layadi* disclose arrangements where only sidewalls are lined. Neither discloses or suggests producing within a dielectric etch chamber, a desired reactive ion etched profile, while using a metallic redeposition to produce a conformal metallic liner on both the sidewalls and the bottom of the etched feature. *Lin* relates to organic low-k dielectric etch and does not disclose or suggest a metallic liner on the sidewalls and bottom of a feature. *Dalton* relates to a method for forming an on-chip decoupling capacitor with bottom hardmask. Again, *Dalton* does not disclose or suggest etching a feature to produce a metal-lined feature where a metallic liner is produced on both the sidewalls and the bottom of the feature. Clearly, none of the cited references of *You*, *Layadi*, *Lin*, and *Dalton*, either singly or in combination, disclose or

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suggest reactive ion etching a low-k dielectric to produce a feature having a metallic liner on both sidewalls and the bottom of the feature. Accordingly, limitations of the independent claims 22 and 24 and claims 3-7, 18 would not be obvious in light of *You* in combination with *Dalton*. In addition, claim 13 would not be obvious over *Layadi* in view of *Lin*, and claims 14, 15, 19 and 20 would not be obvious over *Layadi*.

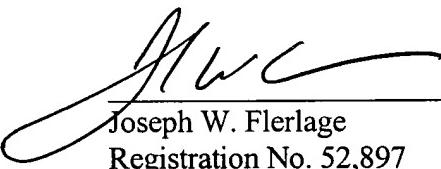
Claims 13 and 25 have been re-written in independent form, and recite structural limitations not disclosed in the cited art, as discussed above for claims 1, 17, 22, and 24. Applicants respectfully request reconsideration of the rejections of the pending claims.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable consideration and allowance for all pending claims. If the examiner believes that a telephone conference would expedite allowance of the application, the examiner is invited to call the undersigned.

Respectfully submitted,

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Joseph W. Flerlage
Registration No. 52,897
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200